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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/801,260
Filing Date: March 15, 2004
Appellant(s): FUJIMORI, ICHIRO

Ognyan Beremski
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 8/15/07 appealing from the Office action mailed 11/28/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

The rejections of claims 1, 8-9, 12 and 14-15 as being unpatentable over Puar et al (U.S. 6,356,497) in view of McCormack et al (U.S. 6,395,591) in Section 2 of the Final Office Action have been withdrawn.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6,403,992	WEI	06-2002
6,395,591	MCCORMACK ET AL.	05-2002
6,356,497	PUAR ET AL.	03-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 8-9, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar et al (U.S. 6,356,497) in view of McCormack et al (U.S. 6,395,591).

This ground of rejection has been withdrawn to simplify the issues to the appeal.

3. Claims 1-10, 12, and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (US. 6,395,591) in view of Puar et al (US. 6,356,497).

Regarding claims 1, 8-9 and 12, McCormack (Fig. 2) discloses a system for reducing noise in a chip (column 2, lines 45-50), the system comprising: a substrate layer 10 integrated within the chip; a transistor well layer 16/18/22 within the chip, which is isolated or shielded from the substrate layer 10 by a shielding layer 12; a transistor 30 of a first transistor type (P type) disposed within the transistor well layer 22, wherein the transistor well layer 22 is coupled to the shielding layer 12, and the shielding layer 12 is disposed between the substrate layer 10 and the transistor well layer 22.

McCormack does not disclose a positive potential of a quiet voltage source coupled to the transistor 30.

However, Puar (Fig. 5) teaches the forming of a system for reducing noise in a chip, the system comprising a transistor of P type disposed in a transistor well layer (N-Well) and having a positive potential Vdd of a quiet voltage source (column 4, lines 59-63) coupled to the transistor. Accordingly, it would have been obvious to couple a positive potential of a quiet voltage source to the transistor well layer (N-Well) of the transistor 30 of McCormack because such coupling of positive quiet voltage source to the transistor well layer would prevent the noise generated from the noisy substrate voltage, as taught by Puar (column 4, lines 55-65).

Regarding claims 2-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16 and coupled to the shielding layer 12, wherein the transistor 28 has a transistor well layer 16 of P type is resistivity coupled to the shielding layer 12 of P type and has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28.

Regarding claim 10, McCormack (Fig. 2) further discloses that the transistor 30 has a transistor well layer 22 of N type is capacitively coupled to the shielding layer 12 of P type.

Regarding claims 14-15, Puar (Fig. 5) also teaches a noisy voltage 38 (column 4, lines 59-63) coupled to the transistor source of a first transistor type (P type).

4. Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al and Puar et al as applied to claim 1 above, and further in view of Wei (US. 6,403,992).

McCormack discloses the shielding layer 12 is deep P-well, but not N-well which is capacitively coupled to the substrate layer 10.

However, Wei teaches the conventional of forming a transistor within a shielding layer of P-well, which is capacitively coupled to the N type substrate (Fig. 3), or a transistor within a shielding layer of N-well, which is capacitively coupled to the P type substrate (Fig. 4). Accordingly, it would have been obvious to form the shielding layer 12 of McCormack with either N type or P type because they both provide the benefits of eliminating substrate effect, as taught by Wei (column 1, lines 47-60).

5. Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei (US. 6,403,992) in view of Puar et al (US. 6,356,497).

Regarding claims 1, 8 and 13, Wei (Fig. 4) discloses a system for reducing noise in a chip, the system comprising: a substrate layer integrated within the chip; a transistor layer 46 integrated within the chip, which is shielded from the substrate layer by a shielding layer N-well 484, wherein the shielding layer N-well 484 reduces the

transfer of noise or body effect in the chip (column 1, lines 55-60); a transistor connected to G4 and having a first transistor type (p type) that couples the transistor layer 46 to the shielding layer 484; and a positive potential Vcc (+5V) of a voltage source coupled to the transistor.

Wei does not disclose that the positive potential Vcc (+5V) is a quiet voltage source.

However, Puar (Fig. 5) teaches a system for reducing noise in a chip, the system comprising a quiet positive potential Vdd (column 4, lines 59-65) coupled to a transistor layer N-well of the P-type transistor. Accordingly, it would have been obvious to connect the positive potential Vcc of the P-type transistor of Wei to a quiet voltage source in order to provide a "quiet" transistor layer which isolates the transistor from the "noisy" substrate voltage, as taught by Puar (column 4, lines 59-65).

Regarding claims 2-7, Wei (Fig. 4) further discloses: a second transistor connected to G3 and having N-type disposed within the transistor layer 46 and resistivity coupled to the N-well shielding layer 484; and a first noisy voltage source GND (0V) coupled to a source S3 of the second transistor type.

Regarding claims 9-10 and 11-12, Wei (Fig. 4) also discloses: the first transistor of P-type disposed within the transistor layer 46 and capacitively coupled to the N-well shielding layer 484; and the N-well shielding layer 484 capacitively coupled to the P-type substrate layer and disposed between the substrate layer and the transistor layer 46.

(10) Response to Argument

ISSUE I - Claims 1, 8-9, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Puar et al (U.S. 6,356,497) in view of McCormack et al (U.S. 6,395,591).

Appellant's arguments on pages 6-11 of Appeal Brief with regarding to the rejections as being unpatentable over Puar in view of McCormack are moot because the rejections over Puar in view of McCormack have been **withdrawn** to simplify the issues to the appeal.

ISSUE II - Claims 1-10, 12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al (U.S. 6,395,591) in view of Puar et al (U.S. 6,356,497).

A. Rejection of Claim 1

- With regarding to the rejection of independent claim 1 as being unpatentable over McCormack in view of Puar (Section 3 of Final Office Action), Appellant (pages 12-14 of Brief) first asserts that the Final Office Action states at pages 2-3 that:

> "However, McCormack (Fig. 2) teaches the forming of a transistor within a transistor well layer and on a lightly doped (p-) substrate layer 50. The transistor well layer is isolated or shielded from the substrate 50 by a p type epitaxy layer 12 disposed therebetween. **The layer 12 functions as a shielding layer for reducing the noise in the chip because it isolates the substrate 10 from the transistor layer and has a higher doping than the underlying substrate 10 for providing immunity**

against parasitic substrate effects or latchup effects (column 1, lines 19-24 and column 4, lines 9-13). Accordingly, it would have been obvious to modify the device of Puar by forming the shielding layer between the substrate layer and the transistor well layer because such forming of the low resistivity shielding layer would isolate the noise transfer to the transistor layer by reducing parasitic substrate effects or latchup effects. (emphasis added)". (see page 13 of Brief).

Appellant then concludes that the combination of McCormack and Puar does not suggest the invention as claimed because "the above bolded statement by the Examiner ... is completely erroneous and is not supported by McCormack" (page 13 of Brief).

Appellant is advised to review the Final Office Action again because the Examiner believes that Appellant is erroneous. Appellant is erroneous because the above cited paragraph of the Final Office Action is in the ground of rejection of Puar in view of McCormack, but not in the ground of rejection of McCormack in view of Puar (Section 3, pages 3-4 of Final Office Action). The Examiner thus submits that Appellant has failed to address the rejection of claim 1 under the ground of rejection of McCormack in view of Puar.

- With further regarding to the rejection of claim 1, Appellant (pages 15-16 of Brief) argues that in Fig. 2 of McCormack, the layer 12 disposed between the substrate 10 and the transistor well layer 16/18/22 would not function as "a shielding layer" for reducing "transfer of noise in the chip".

This argument is not persuasive because of the following reasons:

First, one skill in the art would have no difficulty to recognize that the P-type

layer 12 would function as "a shielding layer" for reducing the noise transfer from the transistor well regions to the substrate 10 because the layer 12 disposed between the substrate 10 and the transistor well regions to isolate the substrate from the well regions. And

Second, Appellant is reminded that in **Fig. 2 of Appellant** below,

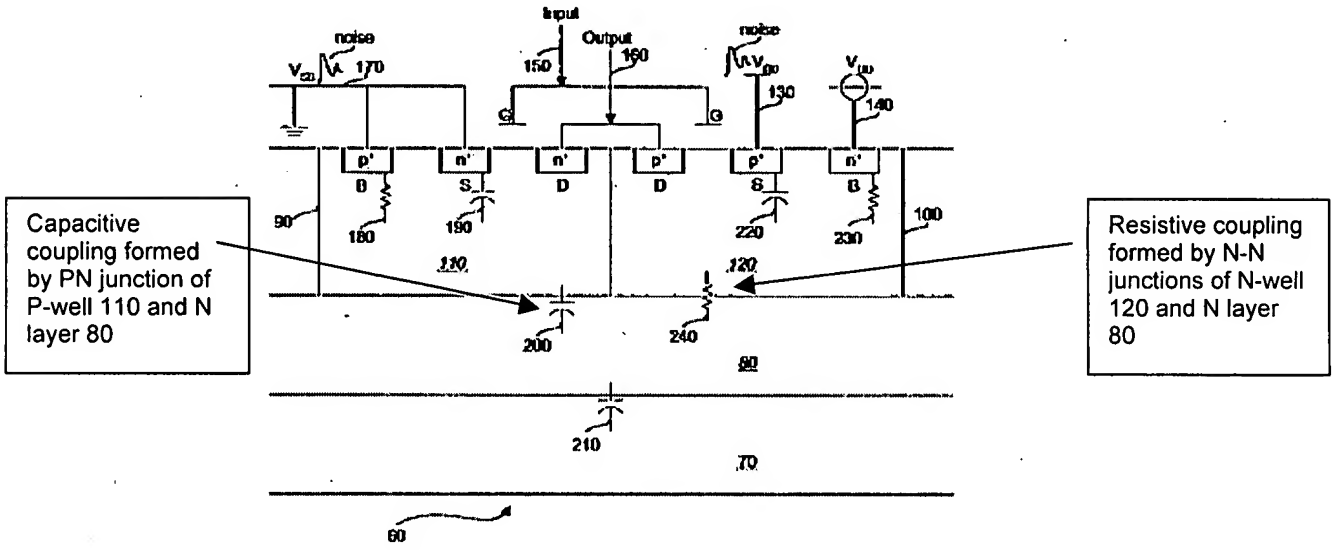


FIG. 2.

The deep N doped layer 80 functions as a shielding layer for reducing the noise in the P-Well 110 and the noise in the N-Well 120 to reach the P-substrate 70 because of the **capacitive coupling 200** formed between the P-Well 110 and the N doped layer 80, and because of the **resistive coupling 240** formed between the N-Well 120 and the N doped layer 80. Specifically, Appellant states at paragraph [20]:

> "For the noise in the p-well 110 to reach the p-substrate 70, the noise may need to pass through two capacitive couplings: a **capacitive coupling 200** between the p-well 110

and the deep n-well 80 and **a capacitive coupling 210** between the deep n-well 80 and the p-substrate 70. Importantly, the capacitive coupling is generally fairly weak, but the capacitive coupling is even weaker when the couplings are placed in series." [emphasis added].

And at paragraph [21]:

"The n-well 120 and the deep n-well 80 may be **resistively coupled 240**. Notably, the deep n-well 80 may provide a substantial amount of resistance to the noise, thereby further reducing any noise propagating through PMOS resistor 100 and reaching substrate 70." [emphasis added].

Now, referring to **Fig. 2 of McCormack** below,

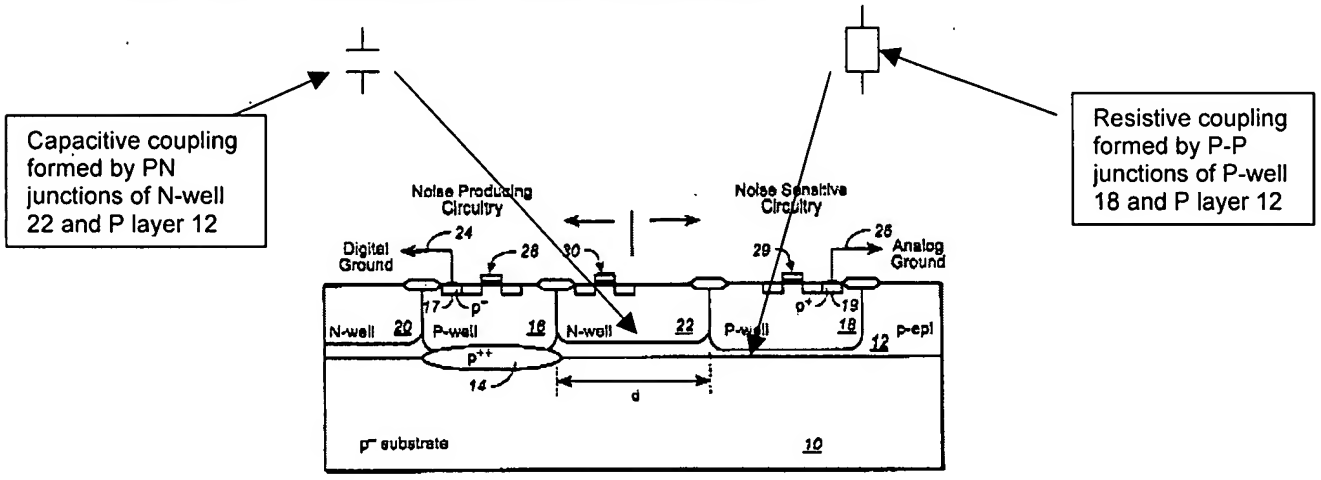


FIG._2

Clearly, Fig. 2 of McCormack also has the **capacitive coupling** formed by **P and N junctions** of the P-doped layer 12 and the N-Well layer 22 and the **resistive coupling** formed by **P and P junctions** of the P-doped layer 12 and the P-Well layer

18. Therefore, the P-doped layer 12 shown in Fig. 2 of McCormack would also function as a shielding layer for reducing the noise in the N-Well 22 and the noise in the P-Well 18 to reach the P- doped substrate 10 because of the junction capacitive coupling formed between the P-doped layer 12 and the N-Well layer 22 and the resistive coupling formed between the P-doped layer 12 and the P-Well layer 18.

Appellant is further reminded that once a reference teaching product appearing to be substantially identical is made the basis of a rejection and the Examiner presents evidence or reasoning tending to show inherency, the burden shifts to Applicant to Applicant to show an unobvious difference. *In re Spada*, 15 USPQ2d 1655, 1658 (Fed. Cir. 1990). In this case, Appellant has failed to provide the evidences to support that the capacitive and the resistive couplings formed by Applicant's N-doped layer 80 would reduce the noise but the capacitive and the resistive couplings formed by McCormack's P-doped layer 12 would not.

B. Rejections of dependent claims 2-3

With regard to the rejections of dependent claims 2-3, Appellant (page 17 of Brief, Section C) has not traverse the rejections of dependent claims 2-3. Therefore, the discussions of the rejection of independent claim 1 in **Section A** above are incorporated herein for reference.

C. Rejection of dependent claim 4

With regard to the rejection of dependent claim 4, Appellant (pages 17-18 of Brief, Section D) argues that "The Examiner is silent as to Applicant's claim 4.

Referring to Figure 2 of McCormack, McCormack does not disclose or suggest that **the 'at least one transistor of said second transistor type is disposed within said transistor layer,'** as recited by the Applicant in claim 4".

Appellant is advised to review the Final Office Action again because with regard to claim 4, the Final Office Action states the following:

> "Regarding claims 2-7, McCormack (Fig. 2) further discloses **a transistor 28 of a second transistor type (N type) disposed within the transistor well layer 16** and coupled to the shielding layer 12, wherein the transistor 28 ..." [emphasis added].

From the statement above, "at least one transistor of said second transistor type" as claimed refers to **"a transistor 28 of a second transistor type (N type)"** shown in Fig. 2 of McCormack, and "said transistor layer" as claimed refers to **"the transistor well layer 16"**. Clearly, the transistor 28 of a second transistor type (N type) is disposed within the transistor well layer 16. Therefore, Appellant's argument is not persuasive because Fig. 2 of McCormack clearly discloses "at least one transistor of said second transistor type is disposed within said transistor layer," as recited by the Appellant in claim 4.

D. Rejection of dependent claim 5

With regard to the rejection of dependent claim 5, Appellant (pages 18-19 of Brief, Section E) argues that Fig. 2 of McCormack does not disclose "said at least one transistor of said second transistor type is resistively coupled to said shielding layer," as claimed.

It is noted that the limitation "said at least one transistor of said second transistor type is resistively coupled to said shielding layer" refers to resistive coupling 180 shown in **Fig. 2 of Appellant below** (also see Applicant's specification, par. [11]), the resistive coupling 180 is formed by P-P junctions of the P-well 110 and the P+ diffusion B and it is resistively coupled to the shielding layer 80 through the P-well 110.

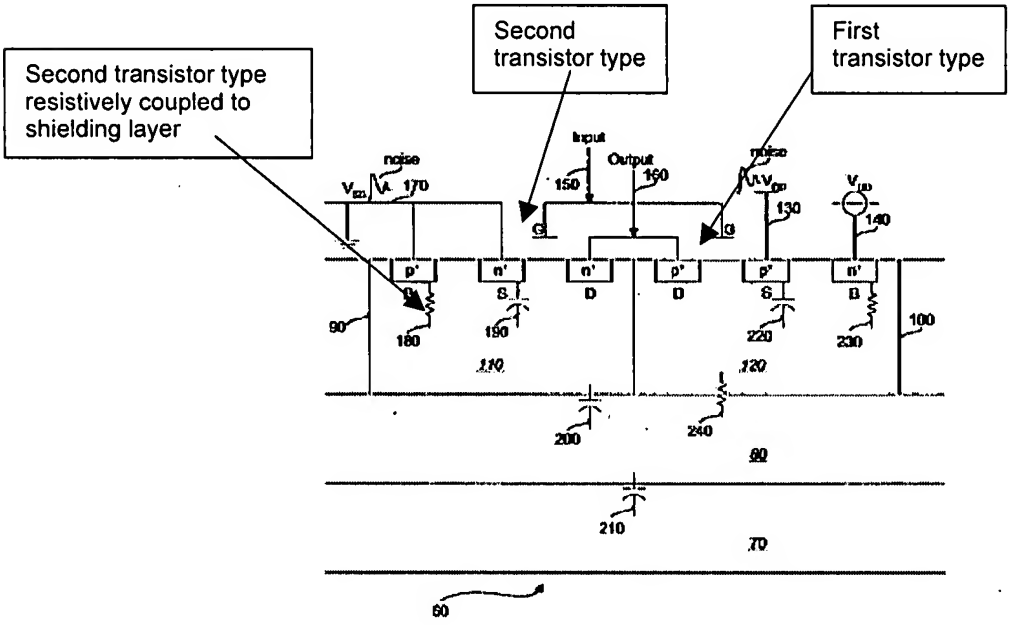


FIG. 2.

Now, referring to **Fig. 2 of McCormack** below,

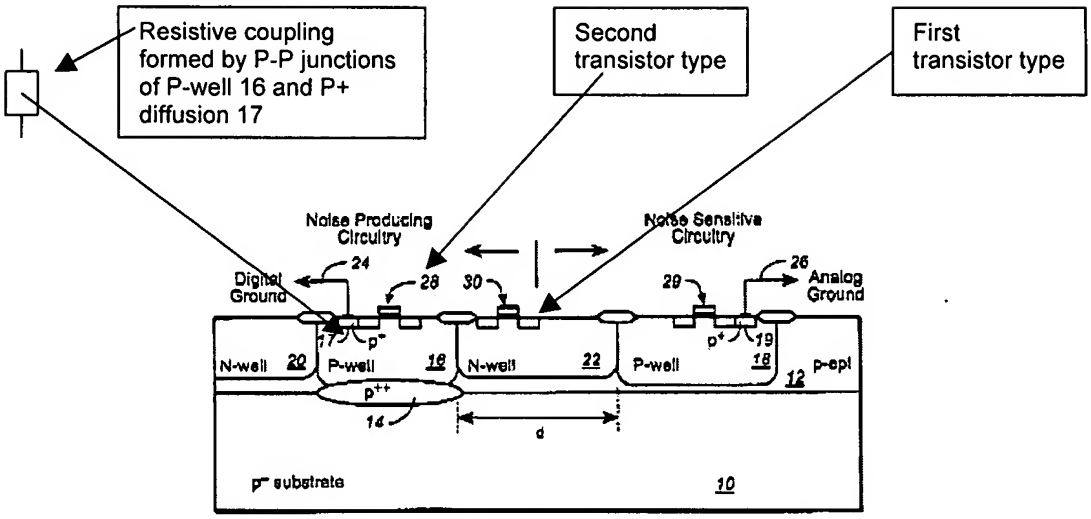


FIG._2

Fig. 2 of McCormack above clearly teaches a resistive coupling which is formed by P-P junctions of the P-well 16 and the P+ diffusion 17 and it is resistively coupled to the shielding layer 12 through the P-well 16. Therefore, Appellant's argument in regard to the rejection of claim 5 is not persuasive because Fig. 2 of McCormack clearly discloses "said at least one transistor [28]of said second transistor type [N type] is resistively coupled to said shielding layer [12]" through the P-well 16.

E. Rejections of dependent claims 6-7

With regard to the rejection of claims 6-7, the Final Office Action states:

"Regarding claims 6-7, McCormack (Fig. 2) further discloses a transistor 28 of a second transistor type (N type) ... has a first noisy voltage source 24 (column 3, lines 53-55) coupled to a source 17 of the transistor 28." (page 4 of Final Office Action)

However, Appellant (pages 19-20 of Brief, Section F) argues that the

terminal 24 coupled to the source 17 of the transistor 28 "is digital ground – it is not a noisy voltage source".

This argument is not persuasive because McCormack clearly states at column 3, lines 53-55 and lines 62-64:

> "Also, the analog ground is sometimes referred to as the 'quiet ground' and the **digital ground is sometimes referred to as the 'noisy ground'** ... , **the digital ground (terminal 24) including ground noise** generated by the n-channel transistors of P-well 16 ..." [emphasis added].

Therefore, the terminal 24 coupled to the source 17 of the transistor 28 is a "noisy" digital ground. Furthermore, as defined by Appellant, a ground is a voltage source. Specifically, Appellant states at paragraph [05], lines 7-8 of specification:

> "A **voltage source** Vss 7 having **a ground** ...";

and at paragraph [15], line 8:

> "A **voltage source** Vss 170 having **an electrical ground**..."

Moreover, Appellant is reminded that in the Office Action mailed on 12/29/2004, the reference issued to Yoo (U.S. 6,724,151) is cited to show that a ground (GND) being defined by one skilled in the art is "a ground voltage source GND" (see "GND" in Fig. 2 of Yoo and column 1, lines 61-64). Therefore, the "noisy ground" terminal 24 coupled to the source 17 of the transistor 28 shown in Fig. 2 of McCormack is "a noisy voltage source" as claimed.

F. Rejection of dependent claim 10

With regard to the rejection of dependent claim 10, Appellant (pages 20-21 of Brief, Section H) argues that Fig. 2 of McCormack does not disclose "said at least one transistor of said first transistor type is capacitive coupled to said shielding layer," as claimed.

It is noted that the limitation "said at least one transistor of said first transistor type is capacitive coupled to said shielding layer" refers to capacitive coupling 220 shown in **Fig. 2 of Appellant below** (also see Applicant's specification, par. [11]), the capacitive coupling 220 is formed by P-N junctions of the N-well 120 and the P+ diffusion S and it is capacitive coupled to the shielding layer 80 through the N-well 120.

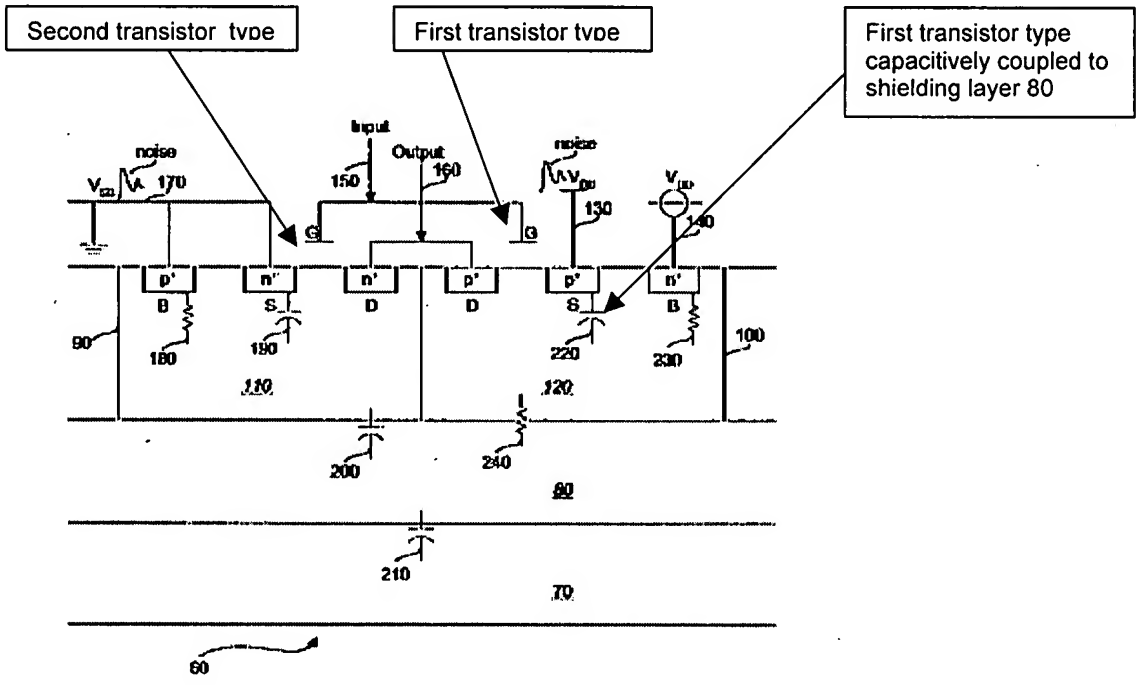


FIG. 2.

Now, referring to **Fig. 2 of McCormack** below,

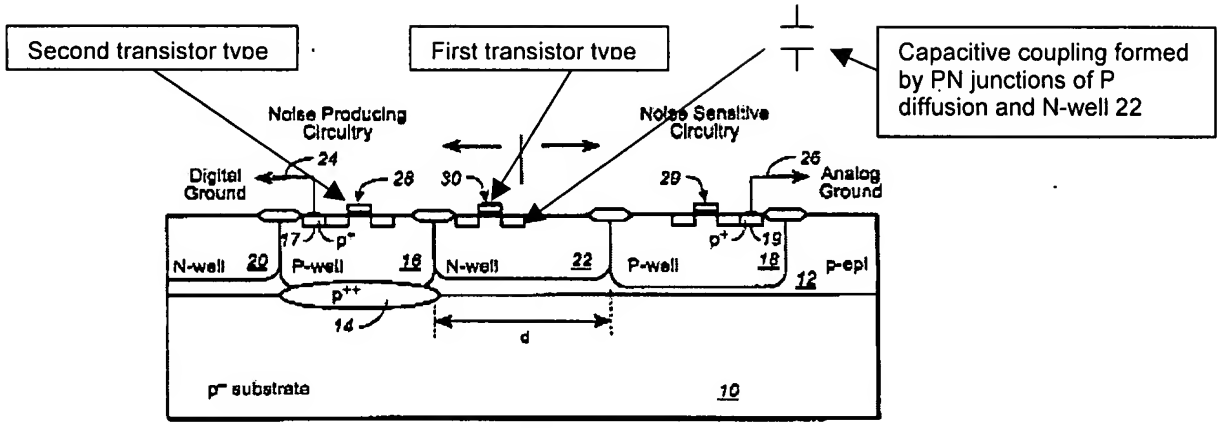


FIG._2

Fig. 2 of McCormack above clearly teaches a capacitive coupling which is formed by PN junctions of the P diffusion and the N-well 22 and it is capacitively coupled to the shielding layer 12 through the N-well 22. Therefore, Appellant's argument in regard to the rejection of claim 10 is not persuasive because Fig. 2 of McCormack clearly discloses "said at least one transistor [30]of said first transistor type [P type] is capacitively coupled to said shielding layer [12]" through the N-well 22.

G. Rejection of dependent claim 12

With regard to the rejection of dependent claim 12, Appellant (page 21 of Brief, Section I) has not traverse the rejections of dependent claim 12. Therefore, the discussions of the rejection of independent claim 1 in **Section A** above are incorporated herein for reference.

H. Rejections of dependent claims 14 and 15

Appellant (page 22 of Brief, Section J) argues that Puar does not suggest "a noisy voltage source coupled to said at least one transistor of a first transistor type" as claimed in claims 14 and 15 because the voltage source 38 shown in Fig. 5 is not "noisy voltage source".

This argument is not persuasive because Appellant has not provide any reasons to support that the voltage source 38 shown in Fig. 5 is not a "noisy voltage source". It is noted that Puar clearly states at column 4, lines 59-63 that VDD shown in Fig. 5 is a "quiet-reference voltage". Therefore, the voltage source 38 is a "noisy voltage source" because it is not connected to "quiet-reference voltage" VDD.

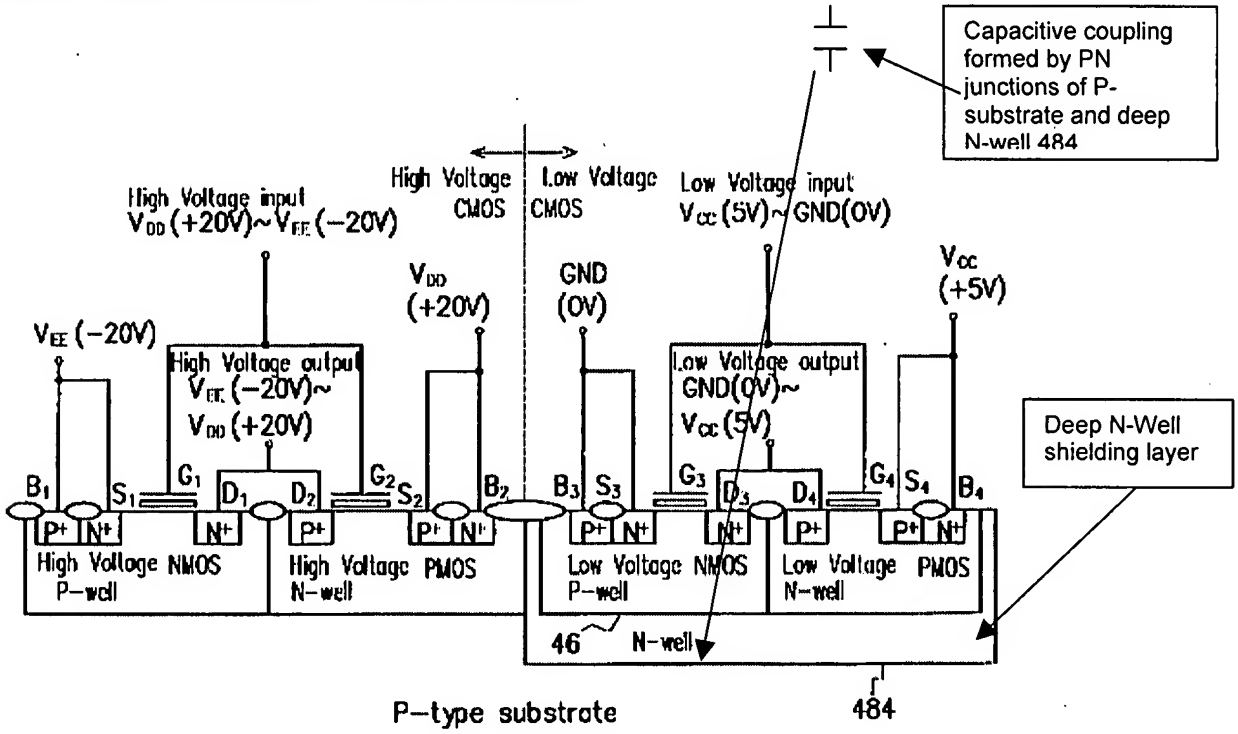
Furthermore, it should be noted that coupling the source of the first transistor to the "noisy" voltage source is not critical. Appellant has failed to point out the criticality of coupling the source of the first transistor to the "noisy" voltage source. There is no evidence of record to indicate that coupling the source of the first transistor to the "noisy" voltage source will achieves an unexpected results. Therefore, the non-criticality of coupling the source of the transistor to the "noisy" voltage source presents strong evidence of obviousness in coupling the source of the first transistor of McCormack to the "noisy" voltage source.

ISSUE III - Claims 11 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over McCormack et al and Puar et al as applied to claim 1, and further in view of Wei (U.S. 6,403,992).

With regard to the rejections of claims 11 and 13, Appellant (page 23 of Brief) argues that it would not obvious to combine Wei with McCormack and Puar because

Wei does not teaches that "said shielding layer is capacitively coupled to said substrate" (claim 11) and "said shielding layer is a deep N-well" (claim 13).

Appellant is advised to review the Wei reference again because **Fig. 4 of Wei below** clearly teaches the features above.



Therefore, Appellant's argument is not persuasive because Fig. 4 of Wei clearly suggests that the shielding layer 484 is a deep N-well and the shielding layer 484 of N type is formed a PN junction with and capacitively coupled to the substrate layer of P type. Thus, Fig. 4 of Wei does suggest the invention as claimed.

ISSUE IV - Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wei (U.S. 6,403,992) in view of Puar et al (U.S. 6,356,497).

A. Rejection of independent claim1

With regard to the rejection of independent claim1, Appellant (pages 24-25 of Brief) argues that Fig. 4 of Wei does not suggest "at least one transistor of a first transistor type that couples said transistor layer to said shielding layer" as claimed because item G4 is not a transistor, it is a ground terminal for the PMOS transistor.

The Examiner recognizes that Appellant is erroneous because in **Fig. 4 of Wei below**, G4 terminal is not relied on for teaching as "at least one transistor of a first transistor type" as asserted by Appellant, but rather, the PMOS transistor (not labeled) connected to terminal G4 is relied on for teaching as "at least one transistor of a first transistor type".

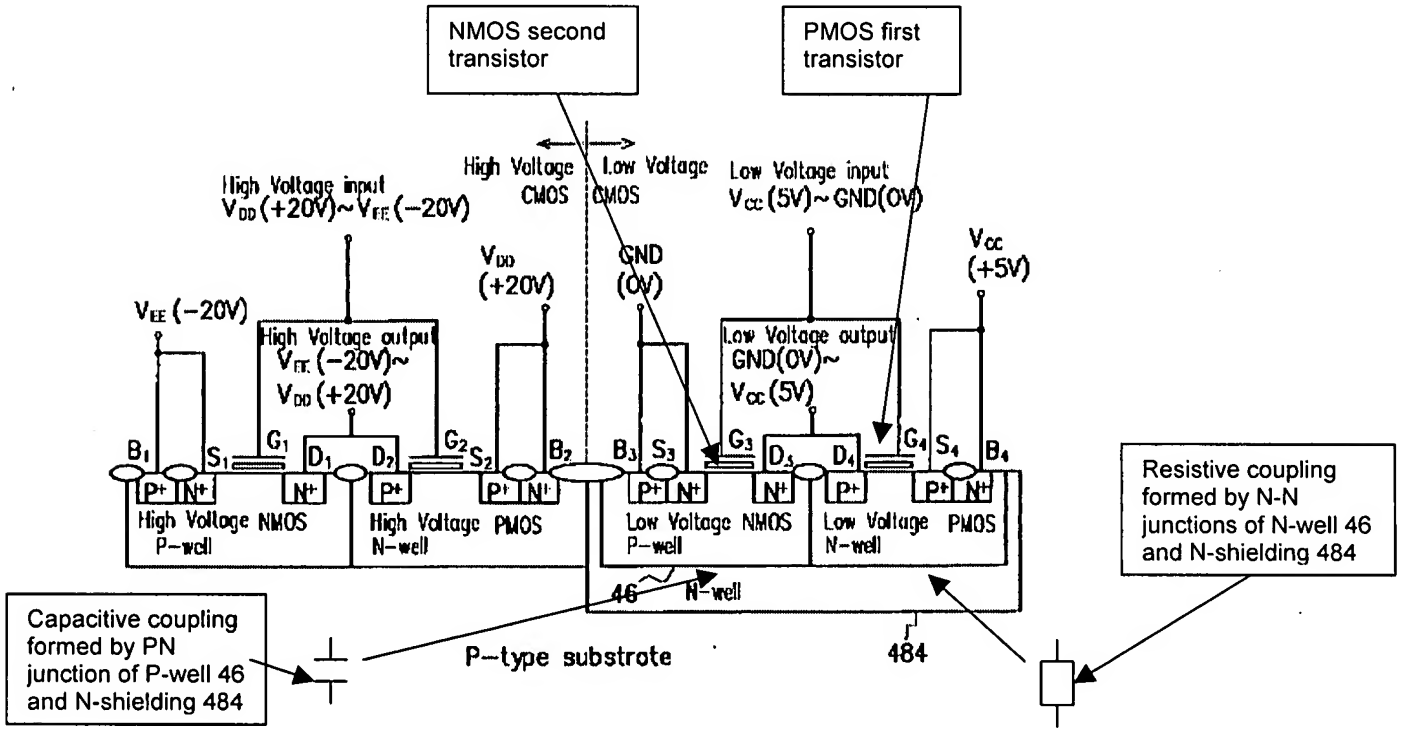


Fig. 4 of Wei above clearly teaches a resistive coupling which is formed by N-N junction of the N-well transistor layer 46 and the N-well shielding 484, and a capacitive coupling is formed by PN junction of the P-well transistor layer 46 and the N-well shielding layer 484. Therefore, Appellant's argument in regard to the rejection of claim 1 is not persuasive because **Fig. 4 of Wei** clearly discloses "at least one transistor of a first transistor type [PMOS] that couples said transistor layer [46] to said shielding layer [484]" as claimed.

B. Rejection of dependent claims 8 and 13

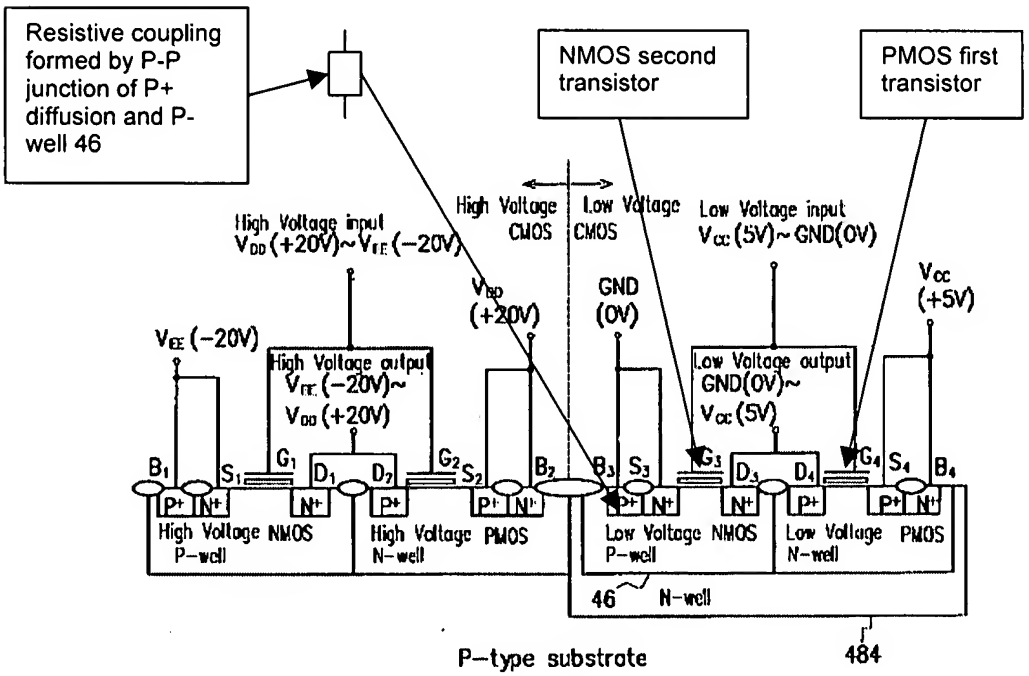
With regard to the rejections of dependent claims 8 and 13, Appellant (page 25 of Brief) has not traverse the rejections of dependent claims 8 and 13. Therefore, the discussions of the rejection of independent claim 1 in **Section A** above are incorporated herein for reference.

C. Rejection of dependent claims 2-7

With regard to the rejections of dependent claims 2-7, Appellant (page 26 of Brief) argues that Fig. 4 of Wei does not suggest "one transistor of said second transistor type is disposed within said transistor layer" (claims 3-4) and "is resistively coupled to the shielding layer" (claims 2 and 5) because item G3 in Fig. 4 is a ground terminal and not a transistor.

The Examiner recognizes that Appellant is erroneous because in **Fig. 4 of Wei below**, G3 terminal is not relied on for teaching as "one transistor of said second

transistor type" as asserted by Appellant, but rather, the NMOS transistor (not labeled) connected to terminal G3 is relied on for teaching as "one transistor of said second transistor type".



It is noted that the limitation "said at least one transistor of said second transistor type is resistively coupled to said shielding layer" refers to resistive coupling 180 shown in **Fig. 2 of Appellant** (also see Applicant's specification, par. [11]), the resistive coupling 180 is formed by P-P junction of the P-well 110 and the P+ diffusion B and it is resistively coupled to the shielding layer 80 through the P-well 110.

Fig. 4 of Wei above clearly teaches the NMOS second transistor type being disposed within the transistor layer 46, and a resistive coupling which is formed by P-P junction of the P+ diffusion and the P-well 46 and it is resistively coupled to the shielding layer 484 through the P-well 46. Therefore, Appellant's arguments in regard to the

rejections of claims 2-5 are not persuasive because Fig. 4 of Wei clearly discloses " one transistor of said second transistor type [NMOS] is disposed within said transistor layer [46]" and "is resistively coupled to said shielding layer [484]" through the P-well 46.

Appellant (page 26 of Brief) further argues that the ground terminal GND of Wei coupled to the source S3 of the NMOS second transistor is not a noisy voltage source (claims 6-7).

This argument is not persuasive because Appellant is reminded that as defined by Appellant, a ground is a voltage source. Specifically, Appellant states at paragraph [05], lines 7-8 of specification:

"A **voltage source** Vss 7 having **a ground** ...";

and at paragraph [15], line 8:

"A **voltage source** Vss 170 having **an electrical ground**..."

It is noted that Appellant has not provide any reasons to support that the voltage source GND coupled to the source S3 of the NMOS is not a "noisy voltage source". One of ordinary skill in the art would recognize that the ground voltage source GND is a "noisy voltage source" because nowhere in the Wei reference states that it is connected to quiet-reference voltage.

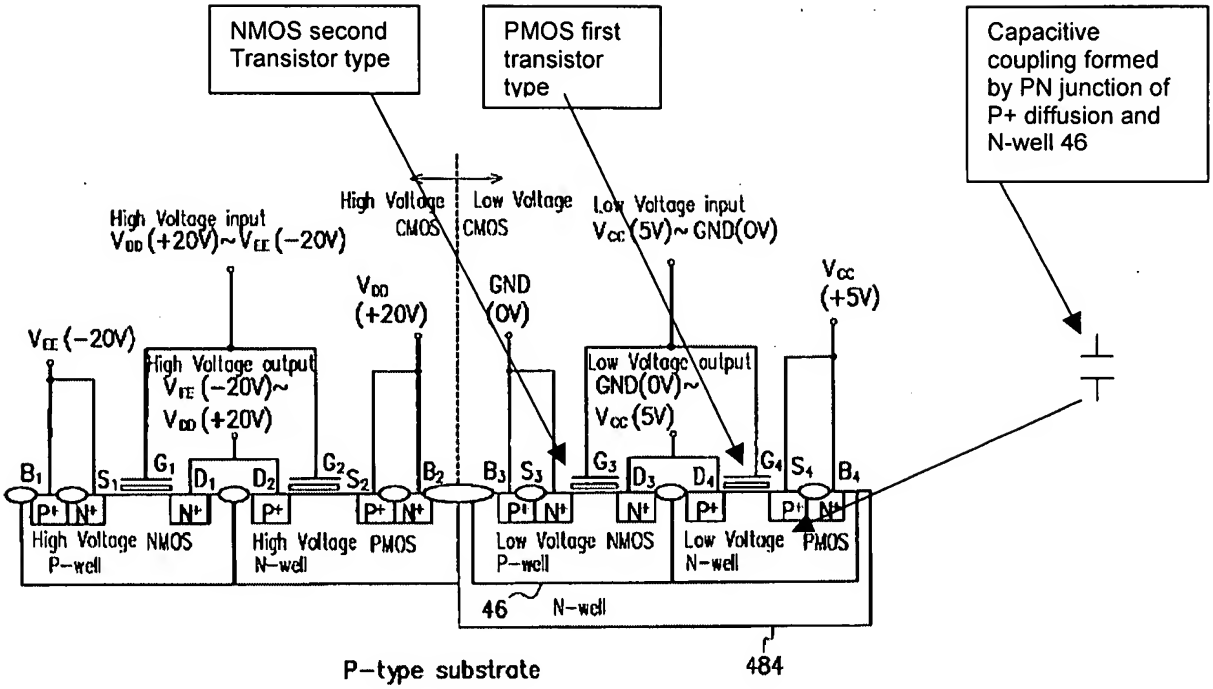
Furthermore, it should be noted that coupling the source of the second transistor to the "noisy" voltage source is not critical. Appellant has failed to point out the criticality of coupling the source of the second transistor to the "noisy" voltage source. There is no evidence of record to indicate that coupling the source of the second transistor to the

"noisy" voltage source will achieves an unexpected results. Therefore, the non-criticality of coupling the source of the transistor to the "noisy" voltage source presents strong evidence of obviousness in coupling the source of the second transistor of Wei to the "noisy" voltage source.

D. Rejection of dependent claims 9-12

With regard to the rejections of dependent claims 9-12, Appellant (page 27 of Brief) argues that Fig. 4 of Wei does not suggest "one transistor of said first transistor type is disposed within said transistor layer" and "is capacitively coupled to the shielding layer" because item G4 in Fig. 4 is a ground terminal and not a transistor.

The Examiner recognizes that Appellant is erroneous because in **Fig. 4 of Wei below**, G4 terminal is not relied on for teaching as "one transistor of said first transistor type" as asserted by Appellant, but rather, the PMOS transistor (not labeled) connected to terminal G4 is relied on for teaching as "one transistor of said first transistor type".



It is noted that the limitation "said at least one transistor of said first transistor type is capacitive coupled to said shielding layer" refers to capacitive coupling 220 shown in **Fig. 2 of Appellant** (also see Applicant's specification, par. [11]), the capacitive coupling 220 is formed by P-N junction of the N-well 120 and the P+ diffusion S and it is capacitive coupled to the shielding layer 80 through the N-well 120.

Fig. 4 of Wei above clearly teaches the PMOS first transistor type being disposed within the transistor layer 46, and a capacitive coupling which is formed by P-N junction of the P+ diffusion and the N-well 46 and it is capacitively coupled to the shielding layer 484 through the N-well 46. Therefore, Appellant's arguments in regard to the rejections of claims 9-12 are not persuasive because Fig. 4 of Wei clearly discloses " one transistor of said first transistor type [PMOS] is disposed within said

transistor layer [46]" and "is capacitively coupled to said shielding layer [484]" through the N-well 46.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

PC

11/13/07

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